MATERIALS ROADMAPS FOR ADVANCED SEMICONDUCTOR DEVICES:
MATERIAL MARKET TRENDS & OPPORTUNITIES

www.Techcet.com
LShonRoy@Techcet.com
KHolland@Techcet.com

L. Shon-Roy
K. Holland, PhD.
February 2015
Disclaimer

- This presentation represents the interpretation and analysis of information generally available to the public or released by responsible agencies or individuals. Data was obtained from sources considered reliable. However, accuracy or completeness is not guaranteed. This report contains information generated by Techcet by way of primary and secondary market research methods.
Outline

- Materials Overview
- Shifts to 3D
- MPU shift to 3D needs for new/more materials
  - Materials Opportunities / Forecasts
- Memory / NVM shift to 3D and impact on materials
  - Materials Opportunities / Forecasts
- Summary
WW Process Materials Forecast

$13B, 2014

Source: Techcet
Forecast of IC Trends by Node and Product Type, includes R&D (200mm equivalent utilized wafers/year)

<table>
<thead>
<tr>
<th>Year</th>
<th>7nm</th>
<th>7nm</th>
<th>3D NAND &gt;150 layers</th>
<th>10-11nm</th>
<th>10-11nm</th>
<th>3D NAND 50 layers</th>
<th>14-16nm</th>
<th>1x-z</th>
<th>22, 14/16nm</th>
<th>2x-z</th>
<th>22-20nm</th>
<th>32, 28, 20nm</th>
<th>32-28nm</th>
<th>45nm</th>
<th>65/45 nm</th>
<th>65 nm</th>
<th>90 nm</th>
<th>130 nm</th>
<th>180-150 nm</th>
<th>&gt;180nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2014</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2016</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2017</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2018</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2019</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2020</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Source: Techcet and SEMI

Leading edge device volumes driven by handheld / portable

Trailing edge device buoyed up by IOT apps
IC Technology Roadmap Evolutions/Revolutions

Note “Node” is “nm” performance, physical is GLph

- **Non-Volatile 1X & 1Z nm**
  - Shrink Planar NAND

- **Non-Volatile 80-30nm features**
  - 3D NAND (BiCS, TCAT, etc.)

  Charge Trap Flash in Vertical Plane
  - also called 3D or V-NAND

  3D/V-NAND Extend for 5+ yrs with
  - 16 to 256 layers

- **DRAM 32-28nm**
  - Vertical Capacitors

- **20nm Planar**
  - SOI Hk/MG

- **14nm TriGate**
  - 14/16nm FinFET-STI

- **10nm**
  - Fin w/ STI, channel change?

- **Non-Volatile <10nm**
  - CNT? PCM

- **RAM & Non Volatile ?**
  - 18-15nm STT-MRAM

- **7nm**
  - III-V or Ge ?

- **EUV**
  - 7nm ?

- **450mm**
  - 7nm?

- **2013**
  - 2014
  - 2015
  - 2016
  - 2017
  - 2018
  - 2019

www.Techcet.com

isnonroy@technce.com
2014 to 2019 Technologies Opportunities

- MPU
  - Multi-patterning Dielectrics will be used for smallest dimension features <28nm
  - High k Gate Dielectric used with Metal Gate Electrode

- DRAM – 1X, 1Z
  - Aggressive scaling, requiring more multipatterning

- Flash
  - 2D - 16nm gates requiring more multipatterning
  - Transition to 3D NAND similar challenges to MPU for 3D structures but with larger design rules, > 20nm.

- More/Better: MP Dielectrics, Cleans, litho, ALD
Advanced Transistor Channel Implications

Technical Challenges

FinFET Formation
- Adequate Hard Mask
- Si Etch Profile for 2 Step-Etch
- Si Fin Surface Roughness & Damage
- Etch Residues
- Post Etch Cleans w/o Defects or Pattern Damage

Uniform “In Situ” Si Fin Doping / Strain
Doping Uniformity Profile Analyses

STI / Gapfill Dielectrics – More Spin on?

Need for More and Better
- Multipatterning Dielectrics and Cleans, selective etchants

Need for More
- Photoresist and ALD processes

Composite from numerous publications with roadmaps

Est. 1st HVM 2014 2016 2018 2020
FinFET with STI and non-implant Si Doping

Ge or III-V? TFET, GAA or STT?
More and More Advanced Cleans ($)

Cleaning Chemicals

$2.5B


Source: Techcet
Source: Techcet Group

www.Techcet.com
lishonroy@techcet.com
Advanced Lithography Implications

Cost, Control & Reproducibility

Without EUV
Sidewall Image Transfer (SIT)
Deposition and Etch-Back Control

Double/Quad Patterning
Multi Litho - incr Dep, Etch, Strip
2-4 X Photoresist Materials
Etch CD Control
Dep Coverage Uniformity
Cleans: Particle and Damage Free
CD, Overlay & Defect Metrology

Directed Self Assembly
Specific Location / Geometry Patterns
Metrology and Defect Analyses before Develop

EUV (first planned for 32nm, now expected <“10nm Node”) Masks Detecting, Controlling & Repairing Defects
Improved Exposure Dose for Throughput
EUV Multi Patterning required for smallest features

# of Photoresist Steps for Critical Layers

Source: Techcet Group

LShonroy@Techcet.com
www.Techcet.com
Feb 2015
Advanced Lithography Implications

Photoresist Critical Layers

EUV not only will allow for finer resolution lithography but aid in reducing the number of litho exposures.

Source: Techcet Group
Hi K /ALD History & Forecast

ALD/CVD High k & Metal Precursors

Source: Techcet
Hi K /ALD Metal Precursors

- 2014 Metal / Metal Oxide Precursors market ~ $225M
- Expected to be ~$400M by 2019
- Front end precursors dominate this space.

Source: Techcet
Advanced MCU Interconnect Challenges/Opportunities

- Cu Resistivity of Smallest Features
  - Thin Effective Barrier Metals
  - CVD Ta self aligned Co?
  - Optimization of Cu Plating to Improve $R_s$

- Ultra Low $\kappa$ & Porous Low $\kappa$
  - Optimized Process & Materials
  - Etch Profiles, Metal Diffusion into dielectric
  - Reduce $\kappa_{\text{eff}}$
  - Adequate Mechanical Strength

Note: There are 8 to 14 Metal Interconnect Levels for MPU. For new interconnect technologies, interconnect levels > 2x transistor process steps.

Composite from numerous publications with roadmaps

TiN intrusion on unsealed porous LowK

www.Techcet.com
- Slurry is the fastest growing segment given that ASPs have held up relative to pad ASPs and Pad lifetime has improved over time.

Source: Techcet
Interconnect Layers and Materials driving CMP Consumables Revenues

- Copper Slurry makes up for >50% of total slurry revenues
- Revenues total ~$1.3B

Source: Techcet
Etch /Dep

Key Challenges for 3D NAND

This way to the Bastille
Non-Volatile Technology Status & Challenges 2014 to ~2018

- 2D NAND is going 3D. Every time they shrink, litho is a problem requiring more multipatterning litho i.e. for 1X and 1Z nodes
  - ~11nm on 2D can now be made w/ 20nm - 30nm on 3D.
- 3D NAND (2014 earliest shipments) --- pressing forward to higher density
  - >30nm lithography
  - Even More aggressive films control
  - Even More aggressive etching techniques
  - Even More defect & process control concerns
  - Challenging defectivity & process control (e.g. etch depth)
## Non-Volatile Technology Roadmap

<table>
<thead>
<tr>
<th>Est. 1st Ship</th>
<th>2014</th>
<th>2015</th>
<th>2016</th>
<th>2017</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Non-Volatile</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1x – 1z NAND</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Non-Volatile >30 nm**

3D NAND (BiCS, V-NAND, TCAT)

**CrossPoint**

RAM & Non Volatile

STT-MRAM? CBRAM? PCM? ReRAM (MVO)?

<10nm

CNT? PCM

Composite from numerous publications with roadmaps

Feb 2015
Material Implications - 3D/ V-NAND

Technical Challenges

from 18 - 32nm layers to 256 - 28nm layers

Etch / Cleans:
Hard Mask for >70:1 Aspect Ratio
Uniform Etch Thru Numerous Layers
Cleans w/o Residues or Defects

Deposition (CVD/ALD):
Difficult High AR Fills Ta$_2$O$_5$, TiN, W
SiO$_2$, Si$_3$N$_4$

Defect Localization / Analysis Critical

NAND Challenge – Low Cost
High Productivity Processes

No new device materials
Ta$_2$O$_5$, SiO$_2$, Si$_3$N$_4$, PolySi, Ta, Ti, W, but
Possibly new cleaning/mixtures and hard
mask materials
Multi-Patterning Precursors: Dielectrics

- Driven by need for finer line widths w/ or w/o EUV

Source: Techcet Group

Source: Techcet

www.Techcet.com
lshonroy@techcet.com
Specialty Gases

- An increase in multi-patterning and interconnect layers drives the need for more electronic specialty gases.
- Total Etch Gases > $180M
- Multi-patterning precursors > $70M
- Low temp precursors for patterning and gapfill being sought after

Source: Techcet
2015 – 2019 Materials Summary

- Increased use of ALD and Hi K / ALD materials although no new materials until 2019 or beyond.
- Increased use of and better gapfill / STI materials
- Multi-patterning will continue through all technology nodes, driving need for
  - better hard mask materials, > 2X in volume in 3yrs
  - Incr. vol. usage of photoresist - 10%+
- Interconnect layers will continue to grow, driving
  - Porous low K
  - More ALD barriers, More CMP Consumables
- Packaging Opportunities – TSV and WLP
Other Materials for 2019 and Beyond?

- **Logic**
  - Transition Si to Higher Mobility Channels at 7nm (less likely at 10nm), i.e. Ge or III-V
  - EUV resists + Multi-Patterning, Directed Self Assembly
  - Higher k Gate Dielectric and Different Metal Gate Electrode

- **Memory**
  - A variety of new materials will be needed to support new device technologies
    - PCM, CNT, STT, ReRAM, RedOx, ...etc.
Where to get more detailed information?

*Techcet’s Critical Materials Report on High k & Metal CVD/ALD Precursors*
Where to get more information on Materials?

www.Techcet.com

- CMP Consumables & Ancillaries
- Gases (Spec. & Bulk)
- ALD / Hi K Metal Precursors
- Photoresists
- ARCs & PR Ancillaries
- Metals – Targets, Conductive Inks/Pastes
- Wafer Mfg Consumables
- Wet Chemicals

- Advanced Cleaning
- Equip’t Consumables -
  - Quartz
  - Graphite
  - Silicon Carbide
  - Ceramics
  - Silicon
- Silicon Wafers/Polysilicon
- Others

Materials Markets, Technology and Supply Chain Expertise
Acknowledgements

- SEMI – H.D. Cho and Dan Tracy, Ph.D.
- VLSI Research - Risto Puhakka
- Sematech - Critical Materials Council
- Techcet Group Analysts
Techcet Group (+ Experience listing)

- Lita Shon-Roy – President / CEO
  - Rasirc/Matheson Gas, IPEC/Athens, Air Products, Rockwell/Brooktree
- Karey Holland, Ph.D. – Chief Technical Officer
  - FEI, NexPlanar, IPEC, Motorola, IBM
- Chris Michaluk – Director of Business Development & Sr. Analyst
  - H.C. Stark, Climax Molybdenum, Williams, Cabot SuperMetals
- Sue Davis – Business Development Manager & Sr. Analyst
  - TI, Sematech, Motorola, Rodel (DOW)
- Bruce Adams – Sr. Technology Analyst
  - Matheson Gas, Air Products, & Chemicals, Honeywell
- Yu Bibby, Ph. D. – Sr. Technology Analyst
  - UV Global, ipCapital Group, Wilkes University
- Jiro Hanaue – Sr. Technology Analyst
  - Applied Materials
- Ralph Butler – Technology Analyst
  - Sun Edison / MEMC, ATMI
- Mike Fury, Ph.D. – Sr. Technology Analyst
  - IBM, Rodel, EKC, Vantage
- Chris Blatt – Sr. Market Analyst
  - Air Products, IPEC/Athens, Zeon Chemicals
Thank you!

LShonroy@Techcet.com
+1-480-382-8336