ALD/CVD High K and Metal Precursors

For Semiconductor Device Process Applications

A TECHCET Critical Materials Report™

Prepared by

J. Sundqvist, Ph.D.
With contributions from K. Holland, Ph.D.
Reviewed and Edited by L. Shon-Roy
TECHCET CA LLC
PO Box 3056
Rancho Santa Fe, CA 92067
www.TECHCET.com
info@TECHCET.com
+1-480-382-8336
RESEARCH METHODOLOGY

TECHCET employs subject matter experts having first-hand experience within the industries, which they analyze. Most of TECHCET’s analysts have over 25 years of direct and relevant experience in their field. Our analysts survey the commercial and technical staff of IC manufacturers and their suppliers, and conduct extensive research of literature and commerce statistics to ascertain the current and future market environment and global supply risks. Combining this data with TECHCET’s proprietary, quantitative wafer forecast results in a viable long-term market forecast for a variety of process materials.

Readers Note: This report represents the interpretation and analysis of information generally available to the public or released by responsible agencies or individuals. Data was obtained from sources considered reliable. However, accuracy or completeness is not guaranteed.
# Table of Contents

1 Executive Summary ........................................................................................................... 9

2 Report Advisory Customers Executive Summary Addendum ..................................... 14
   2.1 Connection Between Equipment Platforms, Precursor Suppliers and Manufacturers ................................................................. 14

3 Scope .................................................................................................................................... 15

4 Introduction to CVD / ALD Processes and Precursors ................................................. 16

5 IC Technology Roadmap and Implications – Device and As-Deposited Material Trends ...................................................................................................... 17
   5.1 Logic Transistor Evolution ...................................................................................... 21
   5.2 Metallization Evolution ......................................................................................... 27
       5.2.1 More than Moore by Interposer and 3D Stacked Packaging Technologies ................. 33
   5.3 Memory Evolution ................................................................................................. 35
   5.4 ALD & materials enabled patterning evolution .................................................... 44
   5.5 Implication of Device Evolution to IC Fabs, Processes and Materials ............... 50
   5.6 Looking Beyond 2022 ......................................................................................... 55
       5.6.1 Moving from 300mm to 450mm Wafers ......................................................... 59
       5.6.2 The Materials Supply Chain .............................................................................. 61
   5.7 Forecast of Wafer Starts by Nodes and Product Mixes by Year ......................... 64

6 High-K/Metal Gate Logic, DRAM & NAND Precursors ............................................. 67
   6.1 Gate Structure Evolution ....................................................................................... 67
   6.2 Application Description and Current Gate Materials .......................................... 68
   6.3 FEOL Logic Metal Precursor Overview ............................................................... 73
   6.4 Future High-k/Metal Gate and Requirements ...................................................... 74
   6.5 High-k capacitor precursor for Memory technologies .......................................... 75
   6.6 High K Current Capacitor materials and precursors .......................................... 78
   6.7 High K Capacitor Market and Forecast ............................................................... 79
   6.8 Long Term Organo Metallics Opportunities 3D Charge Trapping NAND .......... 80
   6.9 High-k / Metal Gate & Capacitor Market and Forecast ....................................... 81
List of Figures

Figure 1: Total ALD / CVD Metal Precursor Market Revenues and Growth ..... 9
Figure 2: A comparison of conformal growth - PVD, CVD vs. ALD. ............... 16
Figure 3: Volume production technology node transitions showing a slowdown starting at 28/22 nm. ................................................................. 17
Figure 4: Some of the known limits of computation, which of many are materials and/or process related. (Nature 512 (2014) 147) ......................... 18
Figure 5: Logic and Memory high-k devices in products by CVD and ALD processes since early 2003 (J. Sundqvist, Baltic ALD 2014). ......................... 19
Figure 6: Paradigm shift from 2D to 3D scaling exemplified by 3D NAND FLASH. ................................................................................................. 20
Figure 7: Selective ALD on Cu over SiO2 surfaces to selectively create a resist layer only on Cu. (ACS Nano, 2015, 9 (9), pp 8710–8717) ............... 21
Figure 8: The High-k / Metal Gate benefit vs. Poly/SiON (GlobalFoundries Semicon Europa 2011) ......................................................................... 22
Figure 9: The evolution of the transistor at Intel from 90 nm to 22 nm...... 22
Figure 10: One of the most highly scaled Poly/SiON transistor technologies, the Qualcomm MSM8960 28 nm LP Snapdragon S3 Transistor Gate - TEM (Chipworks).......................................................................................................................... 23
Figure 11: Comparison of Planar and 3D (TriGate/FinFET) CMOS Transistor. A) ≥ 32 nm Intel, ≥ 20 nm Foundries, B) ≤ 22 nm Intel, ≤ 14/16 nm Foundries, C) ≤ 22 nm Specific foundry customer products, D) ≤ 7 nm Future ........................................................................................................................................... 24
Figure 12: InGaAs on Si wafer by IMEC employing aspect-ratio-trapping technology to create III-V FinFETs on silicon. ......................................................... 25
Figure 13: IMEC logic device roadmap device technology features 2015 down to 5 nm forecasting the stepwise introduction or high mobility channel materials and introduction of a nanowire based transistor architecture. ...... 26
Figure 14: TEM of complete gate-all-around InGaAs Nanowire FET and HRTEM of the gate stack (IEDM 2015, IMEC). Lund University Wrap-gate contacts on vertical nanowires................................................................................. 27
Figure 15: The evolution of metallic wire stacks from 1997 to 2010. Stacks are ordered by the designation of the semiconductor technology node. (C. Alpert of IBM Research) .................................................................................. 28
Figure 16: ITRS Interconnects Roadmap for barriers and conductors (ITRS Summer Meeting July 2015). ...................................................................................... 29
Figure 17: Metal 1 (M1) Process flow: M1 baseline process flow after lithography → mask open → BLok open → copper barrier seed (CuBS) and Fill → CMP (Top) and Via 1, according to Coventor............................................... 30
Figure 18: Metal 2 (V1-M2) baseline process flow after M2-L1 lithography → M2-L2 lithography → V1 partial etch → BLok open and → Cu Barrier Seed and fill (bottom), and CMP, according to Coventor ........................................ 30
Figure 19: ALD and CVD layers for metallization (Hwang et al “Atomic Layer Deposition for Semiconductors” 2014) ................................................................. 31
Figure 20: Intel presenting a thin <2 nm ALD manganese silicate for replacing standard >4 nm TaN barrier leaving additional lateral and vertical space for electroplated Cu lines (Intel, AVS ALD2015, June 2015, Portland, USA). ................................................................................................................................. 32
Figure 21: Complete Co encapsulation of Cu solves two failure modes that leads to shorts in sub 20 nm Cu interconnect. (Applied Materials)........... 33
Figure 22: Micron Hybrid Memory Cube showing stacked DRAM chips on a carrier or logic substrate interconnected by TSV technology............... 34
Figure 23: The forecast of TSV 3D Packaging technologies showing the potential increased growth due to implementation of stacked DRAM products for the smartphone market (Yole, Silicon Saxony Day 2015). .......................... 35

Figure 24: The evolution of the stacked capacitor DRAM memory cell (Hwang et al “Atomic Layer Deposition for Semiconductors” 2014) ............................ 37

Figure 25: Samsung key enabler technologies for DRAM scaling: a honeycomb cell structure (top, left and right) & air-gap spacer (bottom) .................. 40

Figure 26: Non-Volatile Memory Device Roadmap May 2014 Update with the new version from SEMICON Korea 2016 ....................................................... 41

Figure 27: Samsung 3D V-NAND TEM cross section showing the use of a ALD Al2O3 gate dielectric with a TiN/W Metal Gate stack connecting to the vertical charge trapping ONO stack (SiO/SiN/SiO) with a central poly silicon substrate plate connection pillar. (Chipworks) ............................................. 42

Figure 28: ALD Enabled patterning: Representations of process flows in (a) conventional patterning based on lithography and etching, (b) patterning based on lithography and lift-off, (c) area-selective ALD by area-deactivation, and (d) area-selective ALD by area-activation (Kessels et al, Nanoscale, 6 (2014), 10941) .............................................................................................. 45

Figure 29: A high overall selectivity to silicon >35:1 has been achieved using a thin 20nm ALD ZrO2 for 50:1 aspect ratio silicon etch (Fraunhofer CNT). 46

Figure 30: An overview of materials for IC manufacturing that can be etched by chemical ALE (Prof. S.M. George, University of Boulder Colorado) ......... 47

Figure 31: Selective growth, bottom up fill and selective sidewall deposition (Prof. Engstrom, Cornell University) ............................................................. 48

Figure 32: Bottom up patterning via selective growth (T. Younkin, Intel, SPIE February 2015) ..................................................................................... 49

Figure 33: 22nm FinFET Metal Gate Electrode Materials (ref. Chipworks ASMC 2014) ............................................................................................................. 52

Figure 34: In the Applied Materials Olympia chamber pre and post treatments are integrated in a spatial ALD process mode. .............................. 55

Figure 35: Time Line Logic Device Technology through 45 to 5 nm as presented at the More Moore ITRS Stanford Summer Meeting 2015.............. 56

Figure 36: The possible enablers to reduce interconnect resistance beyond 2020 (ITRS Stanford Meeting 2015) ....................................................... 59

Figure 37: G450C tool installation status report as of October 2015 (SEMICON Europa) ........................................................................................ 60

Figure 38: Forecast Silicon Shipment Trends by Node and Product Type (thousands of 200mm equivalent wafers/year)........................................... 66
Figure 39: Schematic diagrams of Intel 22 nm HKMG Tri-Gate P-type MOSFET (PFET) and N-type MOSFET (NFET) showing major performance elements (Tokyo Electron, Materials 7 (2014) 2913) ................................. 67

Figure 40: The 65 nm (Intel) CMOS Poly/SiON Gate Dielectric Structure used for 90nm through to 28nm showing a high resolution TEM cross section of the ~1.2nm SiON gate dielectric. .................................................. 69

Figure 41: Device with High-k first Gate Dielectric Structure, which is a simple evolution from Poly/SiON. ................................................................. 70

Figure 42: Cross sections of 14nm Intel FinFET technology showing pMOS (left) and nMOS (right) ......................................................................................... 71

Figure 43: Planar Devices, Gate-First vs. Gate-Last Replacement Gate technology ..................................................................................................... 73

Figure 44: DRAM Vertical Stacked Capacitor Application sub 65nm. ........ 77

Figure 45: Options for Ferroelectric HfO2, either as a FEIL or BEOL embedded NVM (GlobalFoundries et al, IEDM 2013) ................................. 78

Figure 46: High-k Precursors for Capacitor (DRAM Memory) .................. 80

Figure 47: High-k & Capacitor Metal Precursor Forecast (Logic, DRAM, NAND & Emerging Memory) ................................................................. 83

Figure 48: ALD barrier application replacing PVD barriers for the lower metallization levels ............................................................................. 85

Figure 49: Revenue Forecast for ALD/CVD Metal Gate, Electrodes, Plug Metal (Metal 0), Barrier Precursors & Seeds. ......................................................... 90

Figure 50: Thermal stability of ZyALD™ vs. TEMAZ (www.airliquide.com): Vapor Pressure (left) and Thermal Gravimetric Analysis (TGA, right) .... 95

Figure 51: Total ALD/CVD High-k & Metal Precursor Market development 2013 to 2020 ......................................................................................... 96

Figure 52: High-k / ALD Precursor Supplier Market Share (% of WW Revenues) 2014 ................................................................................................. 100
List of Tables

Table 1: Front End of Line High k and Back End of Line Metal CVD/ALD Precursor Revenues Forecast (M USD/Yr) ................................................................. 10
Table 2: Front End Dielectric Materials & Processes, 2015, 2017 & 2020 .... 12
Table 3: Leading Edge Interconnect Materials & Processes, 2015, 2017 and 2020 .............................................................................................................. 13
Table 4: Expected DRAM releases (Adapted from TECHINSIGHT 2015). ..... 36
Table 5: DRAM scaling, add picture in the development from planar, via cup, deep trench to tubular capacitors ................................................................. 39
Table 6: Memory technologies and material stack for respective technology. .................................................................................................................. 43
Table 7: The Logic transistor and interconnect roadmap as presented at the More Moore ITRS Stanford Summer Meeting 2015................................. 57
Table 8: Dielectric Constant of Transistor Gate and Memory Capacitor Dielectric Material .......................................................................................... 72
Table 9: Metal ALD / CVD precursor used in production for high-k / metal gate stacks .............................................................................................. 74
Table 10: 2013 ITRS Interconnect Difficult Challenges ............................. 88
Table 11: Organometallic Precursors: Synthesizers and Suppliers to the IC Market ..................................................................................................... 98

Appendix

Appendix A: Elements, Background & Producers ........................................... 102